# Quad Voltage Sequencer and Monitor with Programmable Timing

Preliminary Technical Data

# ADM1186

## FEATURES

- Powered from 2.7 V to 5.5 V on the VCC pin
- Monitors four supplies via 0.8% accurate comparators
- Digital core supports up and down supply sequencing and multiple devices may be cascaded (ADM1186-1)
- Four inputs can be programmed to monitor different voltage levels with resistor dividers
- Supply sequencing time delays and a timeout delay to 5% accuracy
- Four open-drain enable outputs
- Open-drain power-good output
- Open-drain sequence complete and bi-directional open-drain Fault pin (ADM1186-1)

## APPLICATIONS

- Monitor and alarm functions
- Up and down power supply sequencing
- Telecommunication and data communication equipment
- PC/servers and notebooks

### Functional Block Diagram

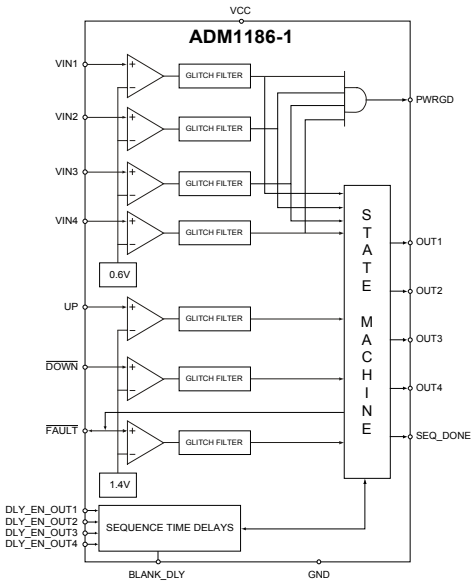



*Figure 1.*

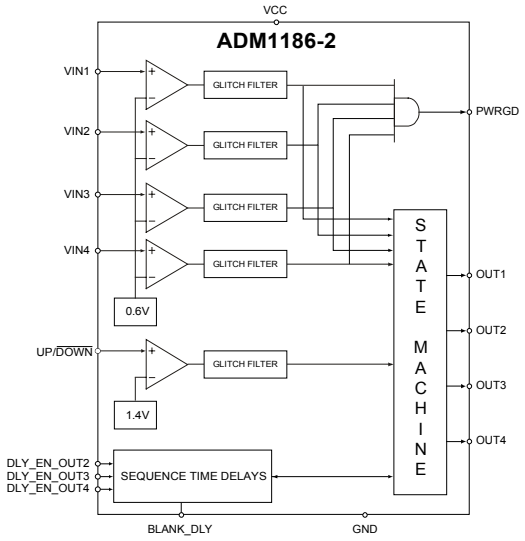



*Figure 2.*

## GENERAL DESCRIPTION

The ADM1186-1 and ADM1186-2 are integrated, four-channel, voltage monitoring and sequencing devices. A 2.7 V to 5.5 V power supply is required on the VCC pin for power.

Four precision comparators monitor four voltage rails, with all comparators sharing a 0.6 V reference and a worst-case accuracy of 0.8%. Resistor networks that are external to the VIN1, VIN2, VIN3, and VIN4 pins set the Under Voltage (UV) trip points for the monitored supply rails.

The ADM1186-1 and ADM1186-2 have four open drain enable outputs, OUTx, that are used to enable power supplies. An open drain power good output, PWRGD, is provided that indicates

**Rev. PrJ**



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

the four VINx inputs are above their UV thresholds.

A state machine monitors the state of the UP and $\overline{\text{DOWN}}$ pins on the ADM1186-1 or the UP/$\overline{\text{DOWN}}$ pin on the ADM1186-2 to control the supply sequencing direction. In the 'Wait Start' state, a rising edge transition on the UP or UP/$\overline{\text{DOWN}}$ pin triggers a power-up sequence. A falling edge transition on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin in the 'Power Up Done' state triggers a power down sequence.

During a power up sequence, the state machine enables each power supply in turn. The supply output voltage is monitored to determine if it rises above the UV threshold level within a user defined duration called the blanking time. If a supply rises above the UV threshold then the next enable output in the sequence is turned on. In addition to the blanking time a user may also define sequencing time delays between each enable output turning on.

When all four enable outputs are on, and the four VINx pins are above their UV trip points the power up sequence is complete. The ADM1186-1 provides an open drain pin, SEQ_DONE, that is asserted high to provide an indication that an up sequence is complete. The SEQ_DONE pins is allows multiple cascaded ADM1186-1 devices to be perform controlled power up and down sequences.

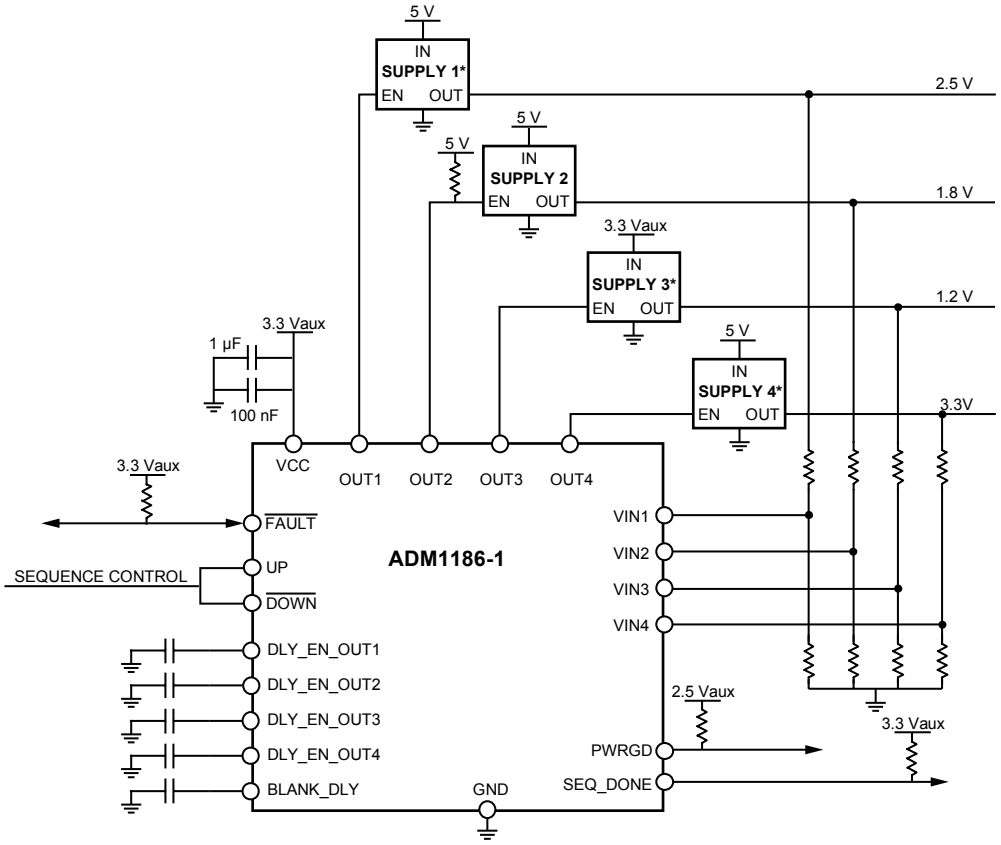
During a power down sequence the enable outputs turn off in reverse order. The sequence time delays between successive supplies the same as during the power up sequence, and no blanking time is used during a power down sequence. At the end of a down sequence the SEQ_DONE pin is brought low.

During sequencing and when powered up, the state machine continuously monitors for any fault conditions. Faults include a UV condition on any of the inputs, or an unexpected control input. Any fault that occurs causes the state machine to enter a fault handler. This immediately turns off all enable outputs, and ensures that the device is ready to start a new up sequence.

The ADM1186-1 has a bi-directional open drain pin, $\overline{\text{FAULT}}$, that facilitates fault handling when using multiple devices. An ADM1186-1 experiencing a fault condition drives the $\overline{\text{FAULT}}$ pin low, causing other connected ADM1186-1devices to enter their own fault handling state..

The ADM1186-1 is available in a 20-lead QSOP package and the ADM1186-2 is available in a 16-lead QSOP package.

## APPLICATION DIAGRAM




*Supplies 1, 3 and 4 include an internal pull to their respective supplies.

*Figure 3.*

## SIMPLIFIED STATE MACHINE DIAGRAM

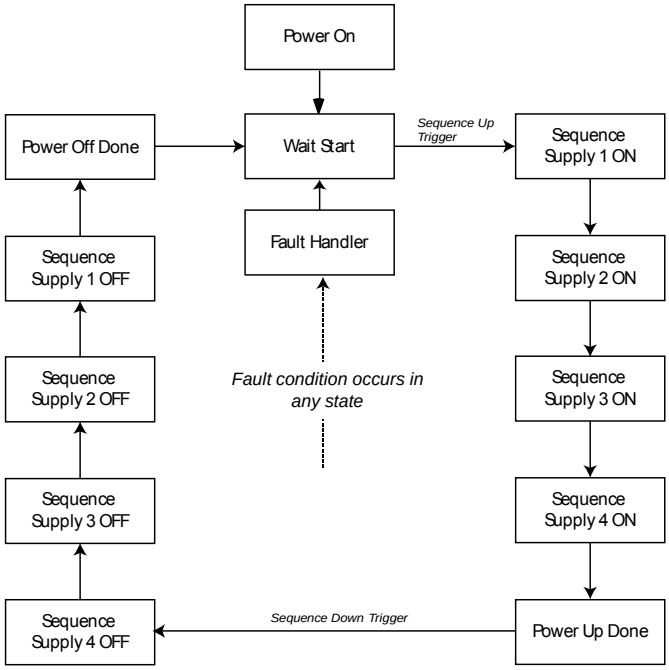



*Figure 4.*

# TABLE OF CONTENTS



## REVISION HISTORY

**Preliminary J – Merged ADM1186 and ADM1187 into single datasheet.**

# SPECIFICATIONS

$V_{VCC}$ = 2.7 V to 5.5 V, $T_A$ = −40°C to +85°C.

**Table 1.**

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| VCC Pin | | | | | |
| Operating Voltage Range, $V_{VCC}$ | 2.7 | 3.3 | 5.5 | V | |
| Supply Current, $I_{VCC}$ | | 130 | 200 | µA | Steady State, Sequence Complete |
| VIN1 to VIN4 (VINx) Pins | | | | | |
| Input Current | −25 | | 25 | nA | $V_{VINx}$ = 0 to 1 V |
| | -100 | | 100 | nA | $V_{VINx}$ = 0 to 5.5 V. $V_{VINx}$ may be greater than $V_{VCC}$ |
| Input Threshold[1] | 0.5952 | 0.6000 | 0.6048 | V | $V_{VCC}$ = 2.7 to 3.6 V |
| | 0.5910 | 0.6000 | 0.609 | V | $V_{VCC}$ = 2.7 to 5.5 V |
| Input Glitch Filter Time[2] | | | | | |
| Low to High | 19.2 | 27.6 | 36 | µs | |
| High to Low | 4.8 | 6.9 | 9 | µs | |
| UP, $\overline{\text{DOWN}}$, and UP/$\overline{\text{DOWN}}$ Pins | | | | | |
| Input Current | −100 | | 100 | nA | $V_{UP/\overline{DOWN}}$ = 0 to 5.5 V. $V_{UP/\overline{DOWN}}$ may be greater than $V_{VCC}$ |
| Input Threshold[1] | 1.379 | 1.4 | 1.421 | V | |
| Input Glitch Filter Time[2] | 4.8 | 6.9 | 9 | µs | |
| DLY_EN_OUT1, DLY_EN_OUT2 to DLY_EN_OUT 4 (DLY_EN_OUT x) and BLANK_DLY Pins | | | | | |
| Time Delay Accuracy | | | 5 | % | For external capacitor values of 10 nF to 2.2 µF. Excludes external capacitor tolerance |
| Time Delay Charge Current | | 14 | | µA | |
| Time Delay Threshold | | 1.4 | | V | |
| Time Delay Discharge Resistor | | 500 | | Ω | |
| OUT1 to OUT4 (OUTx) | | | | | |
| Output Low Voltage, $V_{OUTL}$ | | | 0.4 | V | $V_{VCC}$ = 2.7 V, $I_{SINK}$ = 2 mA |
| Leakage Current | | | 1 | µA | OUTx = 5.5 V |
| $V_{VCC}$ that Guarantees Valid Outputs | 1 | | | V | Output is guaranteed to be either low or giving a valid output level from $V_{VCC}$ = 1 V $V_{OUTL}$ = 0.4 V, $I_{SINK}$ = 100 µA |
| PWRGD Pin | | | | | |
| Output Low Voltage, $V_{PGOUTL}$ | | | 0.4 | V | $V_{VCC}$ = 2.7 V, $I_{SINK}$ = 2 mA |
| Leakage Current | | | 1 | µA | PWRGD = 5.5 V |
| $V_{VCC}$ that Guarantees Valid Outputs | 1 | | | V | Output is guaranteed to be either low or giving a valid output level from $V_{VCC}$ = 1 V $V_{PGOUTL}$ = 0.4 V, $I_{SINK}$ = 100 µA |
| $\overline{\text{FAULT}}$ Pin | | | | | |
| Input Threshold[1] | 1.379 | 1.4 | 1.421 | V | |
| Input Glitch Filter Time[2] | 4.8 | 6.9 | 9 | µs | |
| Output Low Voltage, $V_{FLTOUTL}$ | | | 0.4 | V | $V_{VCC}$ = 2.7 V, $I_{SINK}$ = 2 mA |
| Leakage Current | | | 1 | µA | $\overline{\text{FAULT}}$= 5.5 V |
| $V_{VCC}$ that Guarantees Valid Output | 1 | | | V | Output is guaranteed to be either high or giving a valid output level from $V_{VCC}$ = 1 V $V_{FLTOUTL}$ = 0.4 V, $I_{SINK}$ = 100 µA |
| SEQ_DONE Pin | | | | | |
| Output Low Voltage, $V_{SEQUTL}$ | | | 0.4 | V | $V_{VCC}$ = 2.7 V, $I_{SINK}$ = 2 mA |
| Leakage Current | | | 1 | µA | SEQ_DONE = 5.5V |
| $V_{VCC}$ that Guarantees Valid Output | 1 | | | V | Output is guaranteed to be either low or giving a valid output level from $V_{VCC}$ = 1 V |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | $V_{SEQOUTL}$ = 0.4 V, $I_{SINK}$ = 100 µA |
| TIMING | | | | | |
| VINx to PWRGD | | | | | Includes input glitch filter and all other internal delays |
| Low to High | 20.2 | 28.6 | 37 | µs | $V_{VCC}$ =3.3 V |
| High to Low | 5.8 | 7.9 | 10 | µs | |
| VINx to $\overline{\text{FAULT}}$ and All OUTx low | | | | | Includes input glitch filter and all other internal delays |
| High-to-Low | 5.8 | 7.9 | 10 | µs | $V_{VCC}$ =3.3 V |
| External $\overline{\text{FAULT}}$ to All OUTx low | | | 10 | µs | $V_{VCC}$ =3.3 V |
| Fault Hold Time | 19.2 | 27.6 | 36 | µs | Includes input glitch filter and all other internal delays |

[1] Input comparators do not include hysteresis on their input. The comparator output passes through a digital glitch filter to remove short transients from the input signal that would otherwise drive the state machine.
[2] The input glitch filter time is the combined comparator propagation and digital glitch filter time delay for a comparator overdrive of 50 mV.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VCC Pin | −0.3 V to +6 V |
| VINx Pins | −0.3 V to +6 V |
| UP, $\overline{\text{DOWN}}$, UP/ $\overline{\text{DOWN}}$ Pins | −0.3 V to +6 V |
| DLY_EN_OUTx, BLANK_DLY Pins | −0.3 V to VCC +0.3 V |
| PWRGD, SEQ_DONE, OUTx Pins | −0.3 V to +6 V |
| $\overline{\text{FAULT}}$ Pin | −0.3 V to +6 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature Convection Reflow | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | ≤ 30 sec |
| Junction Temperature | 125°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead QSOP | 149.97 | °C/W |
| 20-Lead QSOP | 125.80 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

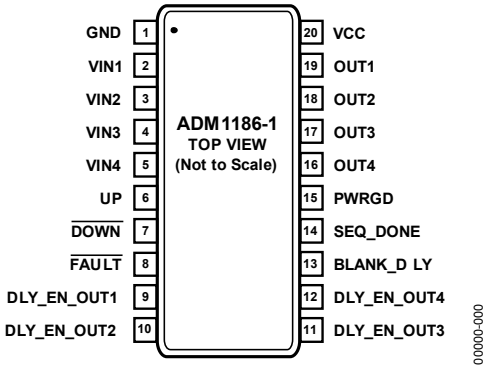



*Figure 5.ADM1186-1 QSOP 20 Pin Configuration*

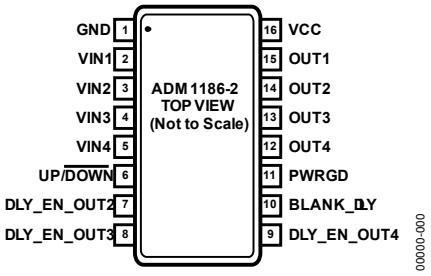



*Figure 6.ADM1186-2 QSOP 16 Pin Configuration*

**Table 4. Pin Function Descriptions**

| ADM1186-1 Pin No. | ADM1186-2 Pin No. | Mnemonic | Description |
|---|---|---|---|
| 1 | 1 | GND | Chip Ground Pin. |
| 2 | 2 | VIN1 | Noninverting Input of Comparator. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core. |
| 3 | 3 | VIN2 | Noninverting Input of Comparator. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core. |
| 4 | 4 | VIN3 | Noninverting Input of Comparator. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core. |
| 5 | 5 | VIN4 | Noninverting Input of Comparator. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core. |
| 6 | - | UP | Noninverting Input of Comparator. A rising edge on this pin initiates a power up sequence when in the WAIT START state. |
| 7 | - | $\overline{\text{DOWN}}$ | Noninverting Input of Comparator. A falling edge on this pin initiates a power down sequence when in the POWER UP DONE state. |
| - | 6 | UP/$\overline{\text{DOWN}}$ | Noninverting Input of Comparators. A rising edge on this pin initiates a power up sequence when in the WAIT START state. A falling edge on this pin initiates a power down sequence when in the POWER UP DONE state. |
| 8 | - | $\overline{\text{FAULT}}$ | Active-Low, Bi-directional, Open-Drain. When an internal fault is detected by the state machine this pin is asserted low by the ADM1186-1 and the SET FAULT state is entered. An external device pulling this pin low also causes the ADM1186-1 to enter the SET FAULT state. |
| 9 | - | DLY_EN_OUT1 | Timing Input. The capacitor connected to this input sets the delay time between the UP input initiating a power up sequence, and OUT1 being asserted high. During a power down sequence this sets the time delay between OUT1 being asserted low, and SEQ_DONE being asserted low. |
| 10 | 7 | DLY_ EN_OUT2 | Timing Input. The capacitor connected to this input sets the delay time between the VIN1 coming into compliance and OUT2 being asserted high during a power up sequence. During a power down sequence this sets the time delay between OUT2 being asserted low and OUT1 being asserted low. |
| 11 | 8 | DLY_ EN_OUT3 | Timing Input. The capacitor connected to this input sets the delay time between the VIN2 coming into compliance and OUT3 being asserted high during a power up sequence. During a power down sequence this sets the time delay between OUT3 being asserted low and OUT2 being asserted low. |
| 12 | 9 | DLY_ EN_OUT4 | Timing Input. The capacitor connected to this input sets the delay time between the VIN3 coming into compliance and OUT4 being asserted high during a power up sequence. During a power down sequence this sets the time delay between OUT4 |

| ADM1186-1 Pin No. | ADM1186-2 Pin No. | Mnemonic | Description |
|---|---|---|---|
| | | | being asserted low and OUT3 being asserted low. |
| 13 | 10 | BLANK_DLY | Timing Input. The capacitor connected to this input sets the blanking time. This is the time allowed between OUTx being asserted and VINx coming into compliance; otherwise, the SET FAULT state is entered. |
| 14 | - | SEQ_DONE | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. When the power up sequence is complete, SEQ_DONE is asserted high. During a power down sequence, the pin remains asserted until the time delay set by DLY_ EN_OUT1 has elapsed. In a fault condition this pin remains asserted high when a fault occurs until the hold time for the fault has elapsed. |
| 15 | 11 | PWRGD | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. The output state of this pin is a logical AND function of the UV threshold state of the VINx pins. When the voltage on all VINx inputs exceeds 0.6 V PWRGD is asserted. This output is driven low if the voltage on any VINx is below 0.6 V. |
| 16 | 12 | OUT4 | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. During a power up sequence, this output is asserted high after the time delay set by the capacitor on DLY_ EN_OUT4 has elapsed. The output is asserted low immediately after a power down sequence has been initiated. |
| 17 | 13 | OUT3 | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. During a power up sequence, this output is asserted high after the time delay set by the capacitor on DLY_ EN_OUT3 has elapsed. During a power down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT4 has elapsed. |
| 18 | 14 | OUT2 | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. During a power up sequence, this output is asserted high after the time delay set by the capacitor on DLY_ EN_OUT2 has elapsed. During a power down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT3 has elapsed. |
| 19 | 15 | OUT1 | Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. During a power up sequence, this output is asserted high after the time delay set by the capacitor on DLY_EN_OUT1 has elapsed (ADM1186-1) or immediately after a rising edge on UP/$\overline{\text{DOWN}}$ (ADM1186-2). During a power down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT2 has elapsed. |
| 20 | 16 | VCC | Positive Supply Input Pin. The operating supply voltage range is 2.7 V to 5.5 V. |

## TYPICAL PERFORMANCE CHARACTERISTICS

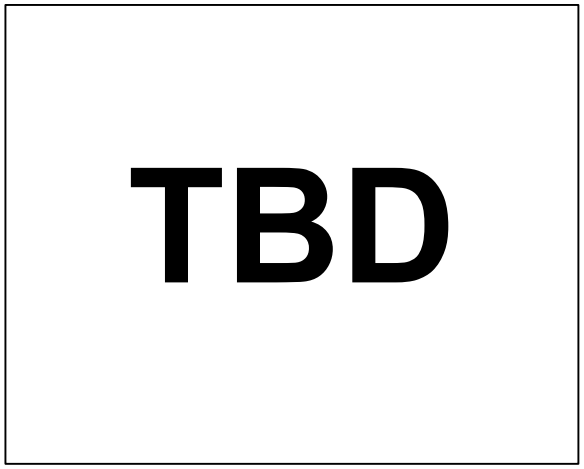



*Figure 7. Supply Current vs. Supply Voltage*

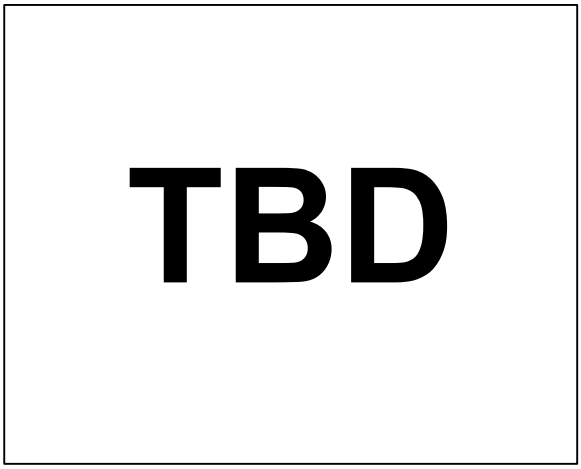



*Figure 8. Supply Current vs. Temperature*

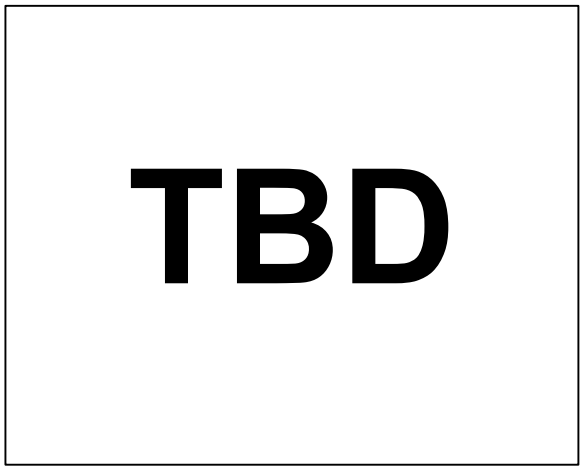



*Figure 9. VINx Trip Threshold Maximum Transient Duration vs. Input Overdrive*

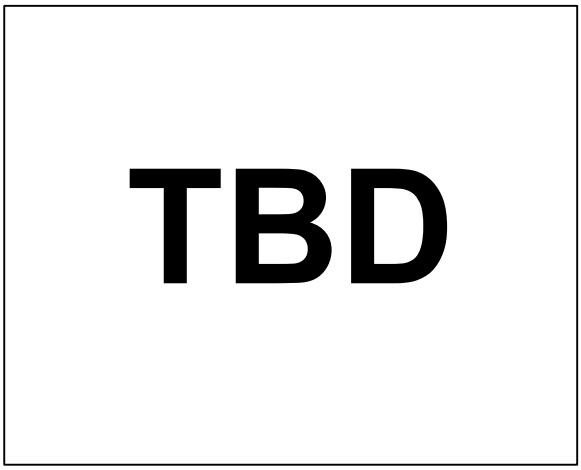



*Figure 10. VINx Trip Threshold vs. Temperature*

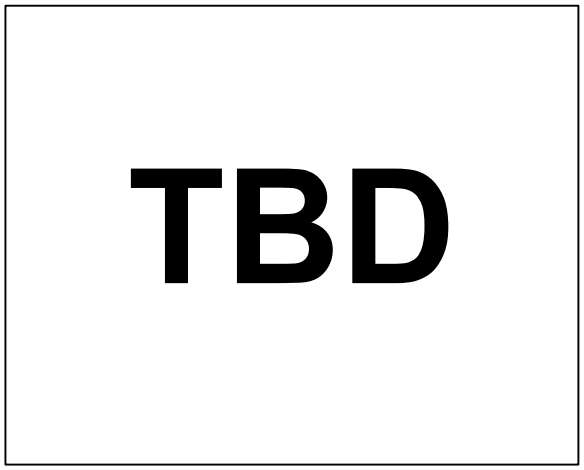



*Figure 11. UP, $\overline{DOWN}$, UP/$\overline{DOWN}$ and $\overline{FAULT}$ Trip Threshold Maximum Transient Duration vs. Input Overdrive*

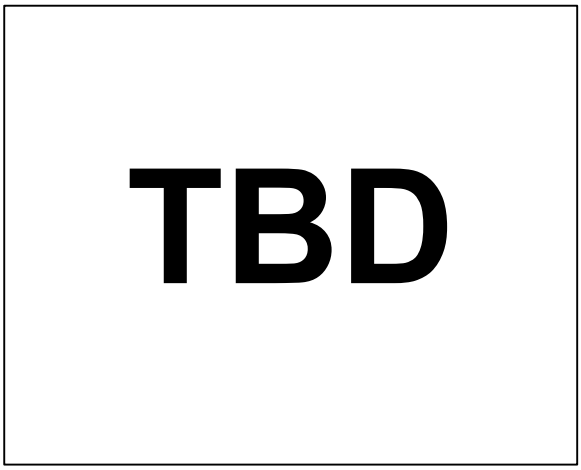



*Figure 12. UP, $\overline{DOWN}$, UP/$\overline{DOWN}$, $\overline{FAULT}$ and Time Delay Trip Threshold vs. Temperature*

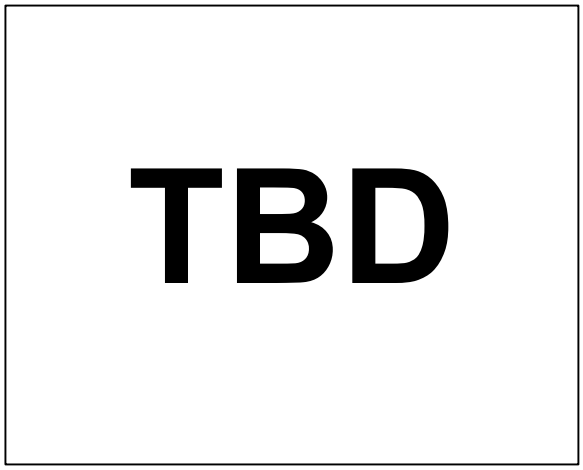



*Figure 13 UP, $\overline{DOWN}$, UP/$\overline{DOWN}$ and $\overline{FAULT}$ Trip Threshold Maximum Transient Duration vs. Temperature*

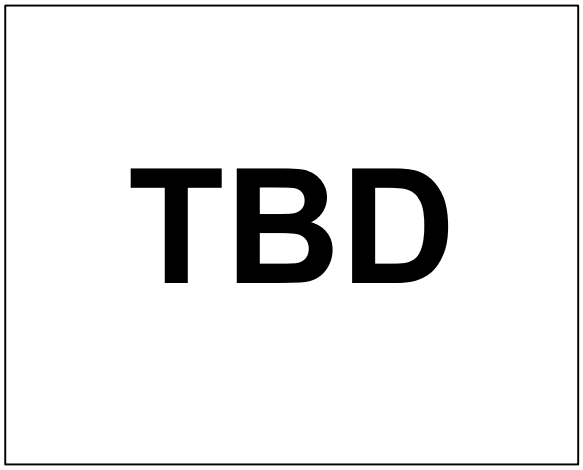



*Figure 14 UP, $\overline{DOWN}$, UP/$\overline{DOWN}$ and $\overline{FAULT}$ Trip Threshold Maximum Transient Duration vs. Supply Voltage*

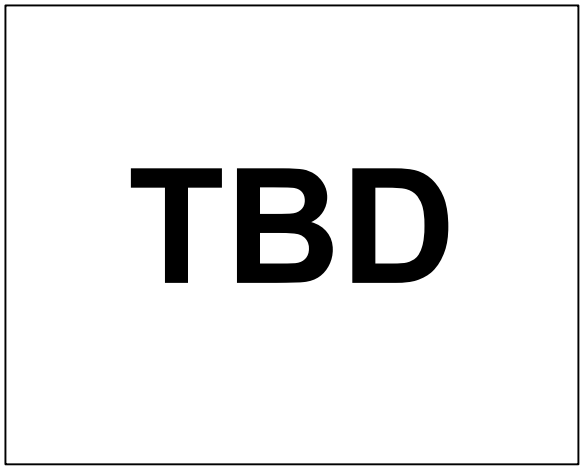



*Figure 15 Time Delay Charge Current vs. Temperature*

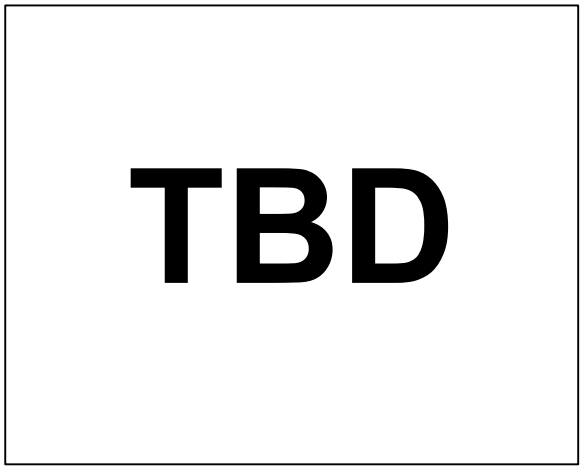



*Figure 16 Output Low Voltage vs. Output Sink Current*

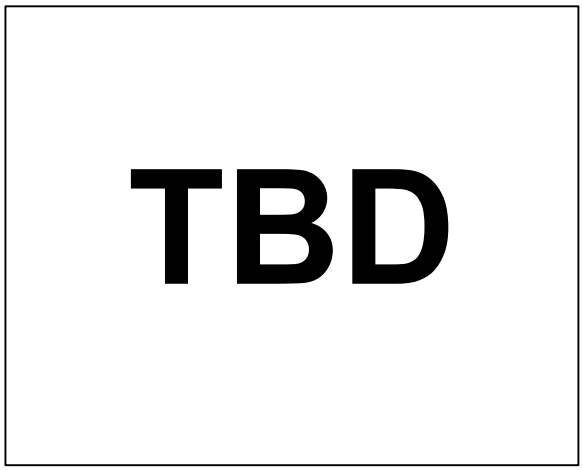



*Figure 17 Output Low Voltage vs. Supply Voltage*

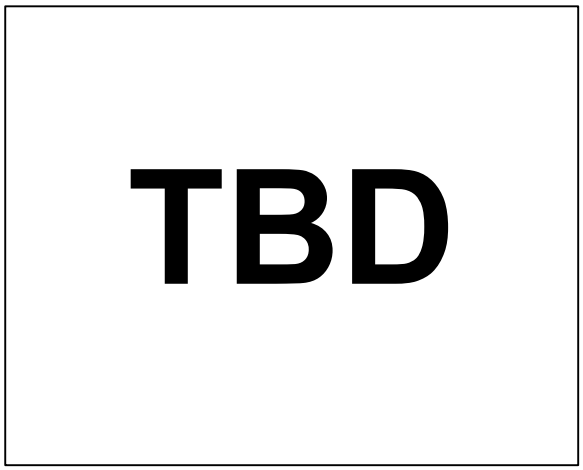



*Figure 18 Delay Time vs. Capacitor Value*

# FUNCTIONAL DESCRIPTION

The operation of the ADM1186 is described in the following sections. Where differences exist between the ADM1186-1 and ADM1186-2 these are noted where necessary. Detailed functional block diagrams of the ADM1186-1 and ADM1186-2 are shown in Figure 20 and Figure 22 respectively.

The ADM1186 operation is explained in the context of a typical voltage monitoring and sequencing application, as shown in Figure 3. This example uses the ADM1186-1, as it is essentially a superset of the functionality of the ADM1186-2. In this application, the ADM1186-1 turns on four regulators, monitors four separate voltage rails, and generates a power-good signal to turn on a microcontroller when all power supplies are on and above their UV threshold level.

Figure 24 shows a typical ADM1186-2 voltage sequencing and monitoring application.

## POWER UP SEQUENCING AND MONITORING

The main supply (in this case 3.3 V) powers up the device via the VCC pin as the voltage rises. A supply voltage of 2.7 V to 5.5 V is required to power the device.

The state machine core of the ADM1186 remains in the WAIT START state following power up. A rising edge on the UP pin initiates a power up sequence moving the state machine to the DELAY 1 state. The ADM1186-2 does not have a DLY_EN_OUT1 pin, and so it omits the DELAY1 state. Figure 1Figure 21 shows the ADM1186-1 state machine in detail, Figure 23 provides the same for the ADM1186-2.

In the DELAY1 state a time delay, set by the capacitor on DLY_EN_OUT1 is allowed to elapse. Then in the ENABLE OUT1 state the OUT1 pin is asserted high. OUT1 is an open-drain active high output, and in this application enables the output of a 2.5 V regulator.

During the ENABLE OUT1 state the VIN1 pin starts to monitor the 2.5 V supply after a blanking delay, set by the capacitor on BLANK_DLY. The blanking delay, which is the same for all supplies, is set to allow the slowest rising supply sufficient time to switch on.

An external resistor divider scales the supply voltage down for monitoring at the VIN1 pin. The resistor ratio is chosen so that the VIN1 voltage is 0.6 V when the supply voltage rises to the UV level at start-up (a voltage below the nominal 2.5 V level). In this case, R1 is 7.4 kΩ, and R2 is 2.5 kΩ, so a voltage level of 2.375 V corresponds to 0.6 V on the noninverting input of the first comparator.

If the output of the 2.5 V regulator meets the UV level when the blanking time elapses then the state machine continues the power up sequence moving into the DELAY 2 state. A time delay, set by the capacitor connected to the DLY_EN_OUT2 elapses before turning on the next output enable, OUT2, in the ENABLE OUT2 state.

If the 1.8 V supply does not rise to the UV level before the blanking time elapses then sequencing immediately stops and the state machine enters the SET FAULT state.

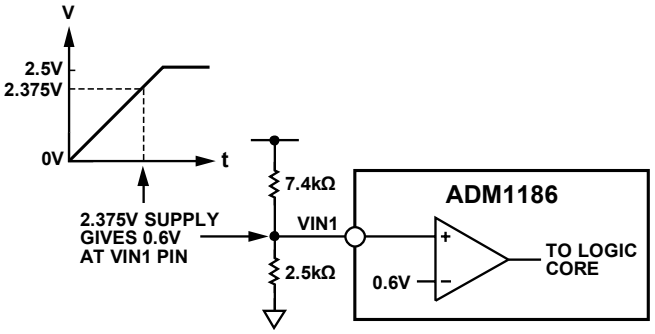



*Figure 19. Setting the Under Voltage Threshold with an External Resistor Divider*

The same scheme is implemented with the other output and input pins. Every supply turned on via an output pin, OUTx, is monitored via an input pin VINx to check that the supply has risen above the UV level within the blanking time before moving onto the next supply.

Once a supply is on and operating correctly, the ADM1186 continues to monitor it for the duration of the power up sequence. If any supply drops below its UV threshold level during a power up sequence then sequencing stops, and the state machine enters the SET FAULT state.

A falling edge on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin when the state machine is in the WAIT START state or at any time during a power up sequence generates a fault.

The PWRGD pin asserts high, independently of the state machine, when all four VINx pins are above their UV threshold. The state machine in the ADM1186-1 indicates the power up sequence is complete by asserting the SEQ_DONE pin high.

## OPERATION IN POWER UP DONE STATE

When the power up sequence is complete, the state machine remains in the POWER UP DONE state until one of four things happen:

- An Under-Voltage condition occurs on one or more of VIN1 to VIN4 generating a fault
- A falling edge occurs on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$pins initiating a power down sequence
- A rising edge occurs on the UP pin generating a fault (ADM1186-1 only)
- An external device brings the $\overline{\text{FAULT}}$ pin low causing a fault (ADM1186-1 only)

Figure 25 and Figure 26 are waveforms that highlight the behavior of the ADM1186 under various fault situations during the POWER UP DONE state.

## POWER DOWN SEQUENCING AND MONITORING

When the ADM1186 is in the POWER UP DONE state a falling edge on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin initiates a power down sequence.

The state machine moves to the DISABLE OUT4 state, bringing the OUT4 pin low, and switching off the 1.0 V regulator. A time delay set by the capacitor on the DLY_EN_OUT4, elapses before the state machines moves to the DISABLE OUT3 state.

This sequence of steps repeats until all four regulators are switched off, and the device is in the WAIT START. As the ADM1186-2 does not have a DLY_EN_OUT1 pin, there is no delay between the OUT1 pin being brought low and the state machine returning to the WAIT START state. Once in the WAIT START state the SEQ_DONE pin is brought low.

During a power down sequence, the state machine monitors the supplies that are still on. If a supply drops below its UV threshold before it is turned off the power down sequence immediately stops and the state machine enters the SET FAULT state.

A rising edge on the UP or UP/$\overline{\text{DOWN}}$ pin during a power down sequence generates a fault.

The PWRGD pin asserts low, independently of the state machine power down sequence, when any one or more of the VINx pins drops below 0.6 V.

## FAULT CONDITIONS AND HANDLING

During supply sequencing and operation in the POWER UP DONE state the ADM1186 is continuously monitoring the VINx, UP, $\overline{\text{DOWN}}$ and UP/$\overline{\text{DOWN}}$ pins for fault conditions. The $\overline{\text{FAULT}}$ pin on the ADM1186-1 is monitored to detect external faults generated by other devices, which is important during cascade operation.

The following are internally generated faults:

- A supply fails to reach the UV threshold within the time defined by the BLANK_DLY capacitor during a power up sequence
- A UV condition occurs on VINx after the blanking time has elapsed during a power up sequence
- A UV condition occurs on VINx before the supply is disabled during a power down sequence
- A falling edge occurs on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin during a power up sequence or the WAIT START state
- A rising edge occurs on the UP or UP/$\overline{\text{DOWN}}$ pin during a power down sequence or the POWER UP DONE state

The action taken by the state machine in the ADM1186 is the same regardless of whether the fault is internal or external. The state machine enters the SET FAULT state and asserts the $\overline{\text{FAULT}}$ pin low (ADM1186-1 only) and all four OUTx enable pins low.

The ADM1186 remains in the SET FAULT state for the fault hold time before moving into the CLEAR FAULT state. In CLEAR FAULT the state machine waits for the UP or UP/$\overline{\text{DOWN}}$ pin to be low. If the UP or UP/$\overline{\text{DOWN}}$ pin is brought low while in the CLEAR FAULT state, it must remain low for the glitch filter time in order for it to be recognized as being low. On the ADM1186-2 when the UP/$\overline{\text{DOWN}}$ pin is low the WAIT ALL OK state is entered.

When the ADM1186-1 is in the CLEAR FAULT state and the UP pin is low the WAIT ALL OK state is entered and the $\overline{\text{FAULT}}$ pin is de-asserted. If an external device is driving the $\overline{\text{FAULT}}$ pin low, the state machine remains in the WAIT ALL OK state until the $\overline{\text{FAULT}}$ pin returns high. The state machine then transitions into the WAIT START state, ready for the next power up sequence.

## DEFINING TIME DELAYS

The ADM1186 provides the ability to define sequence and blanking time delays using capacitors. The ADM1186-1 has four DLY_EN_OUTx pins, while the ADM1186-2 has three DLY_EN_OUTx pins. Capacitors connected to these pins control the time delay between supplies turning on and off during the power up and down sequences. Both devices provide one pin to set the blanking time delay.

The ADM1186-1 provides a pin called DLY_EN_OUT1 that the ADM1186-2 does not. The capacitor on this pin sets the time delay used before enabling OUT1 during a power up sequence, and the delay after disabling OUT1 during a power down sequence. While this time delay is not essential when a single ADM1186-1 device is used, it is essential when multiple devices are cascaded.

When the ADM1186-1 devices are used in cascade, the capacitor on DLY_EN_OUT1 sets the time delay between the power up and power down between supply 4 on device N and supply 1 on device N+1.

During the power on sequence, the capacitor sets the time from the end of the blanking period allowed for a supply to rise above the UV threshold to the next output enable being asserted high. During the power down sequence the capacitor sets the time between consecutive output enables being asserted low.

The blanking time is controlled by the capacitor on the BLANLK_DLY pin. This capacitor sets the time allowed between an output enable being asserted and the supply turning on and rising above its defined UV threshold.

A constant current source is connected to a capacitor through a switch that is under the control of the state machine. This charges a capacitor until the threshold voltage is reached. For all capacitors the duration of the time delay is controlled by the following formula

$$T_{DELAY} = C_{DELAY} \times 0.1$$

Where:

$T_{DELAY}$ is the time delay in seconds

$C_{DELAY}$ is the capacitor value in μF.

For capacitor values of 10 nF to 2.2 μF the timing range is therefore 1 ms to 220 ms. If a capacitor is not connected to a timing pin then the time delay is minimal, of the order of microseconds.

When a capacitor is not being charged by the current source, it is connected via a resistor to ground. Each capacitor has a dedicated resistor, with a typical value of 500 Ω. In order to ensure accurate time delays this means that time must be allowed after a capacitor has been used for it to discharge. Typically allowing five RC time constants for the capacitor to discharge is sufficient to less than 1% of the threshold voltage.

There are a number of instances where the time delays may not be accurate. These occur when insufficient time is not allowed for a capacitor to discharge. These instances include, but are not limited to, the following:

- If a power down sequence is initiated a short time after entering the POWER UP DONE state
- A fault occurs in the ENABLE OUT1 state when the BLANK_DLY capacitor is charged and a power up sequence is started again quickly afterwards
- The DLY_EN_OUTx delay time is very short and insufficient to allow the BLANK_DLY capacitor to fully discharge

In order to achieve the best timing accuracy over the operational temperature range the choice of capacitor is critical. Capacitors are typically specified with a value tolerance of ±5 %, ±10% or +/20%, but in addition to the value tolerance there is also a variation in capacitance over temperature.

Where high accuracy timing is important the use of capacitors that use a C0G, sometimes called NPO, dielectric will result in a capacitance variation of only ±0.3 % over the full temperature range. This contrasts with typical variations of ±15 % for X5R, X7R and ±22 % for X7S capacitor dielectrics.

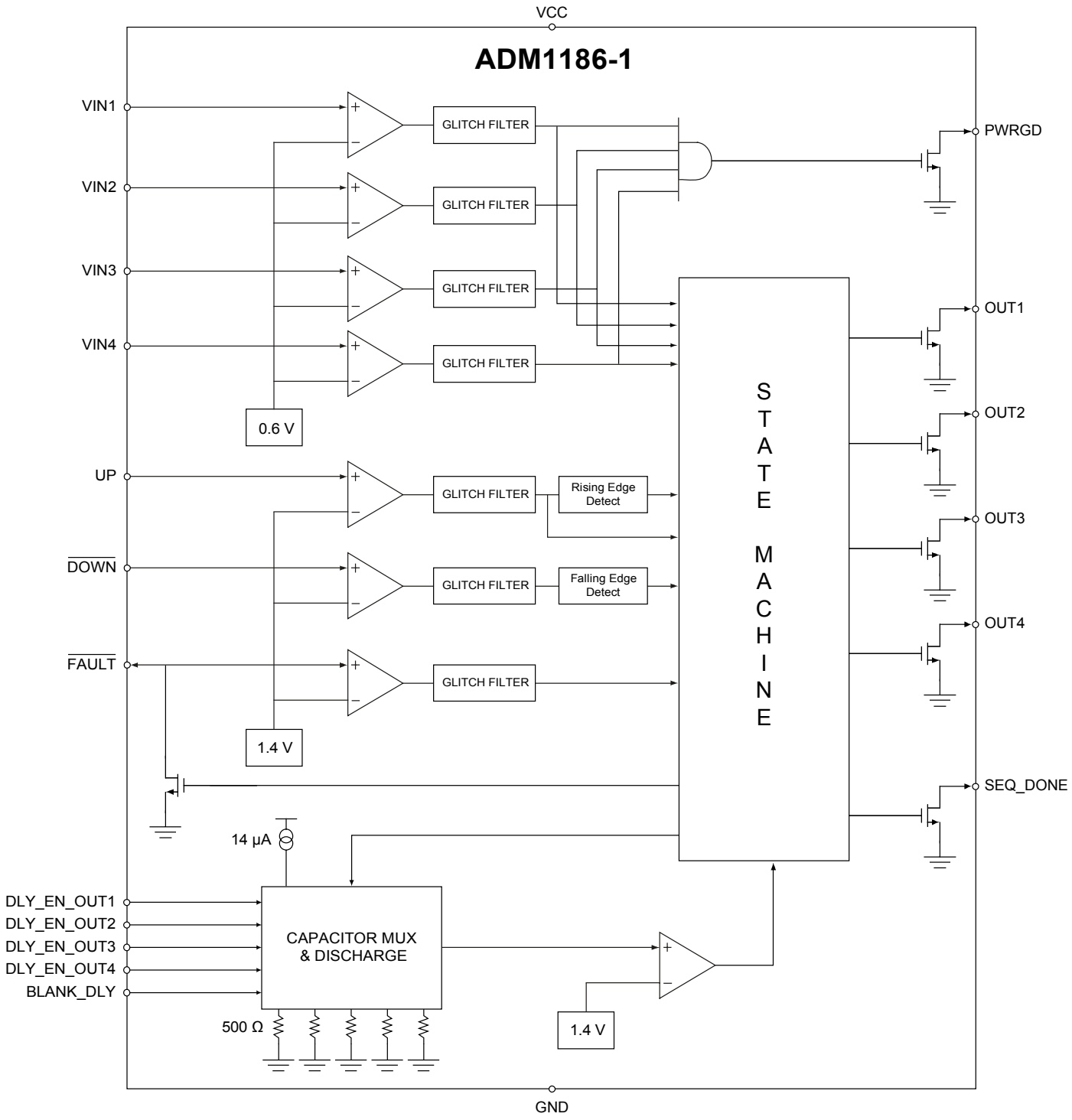



*Figure 20. Functional Block Diagram of the ADM1186-1*

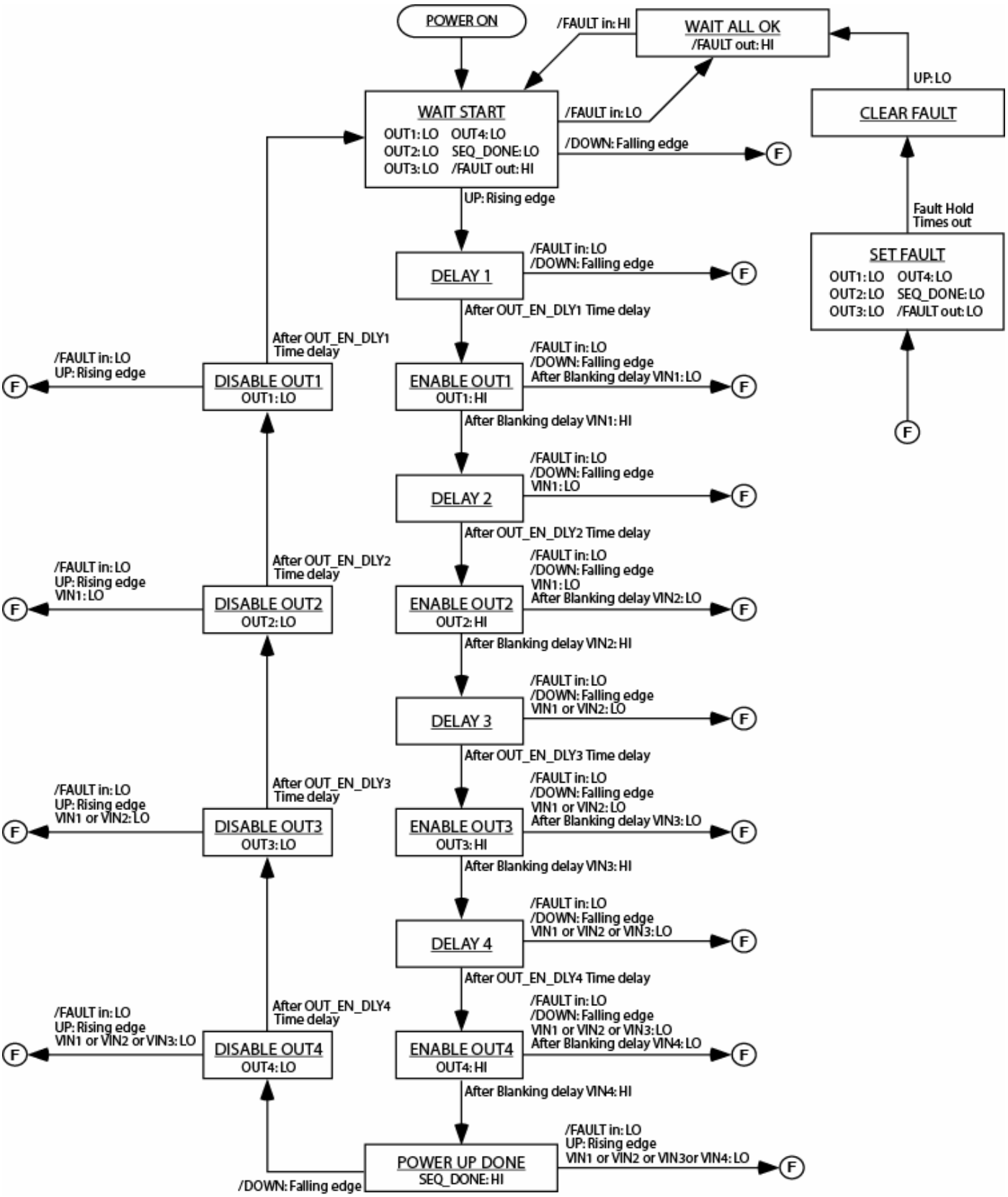



*Figure 21. ADM1186-1 State Machine Operation*

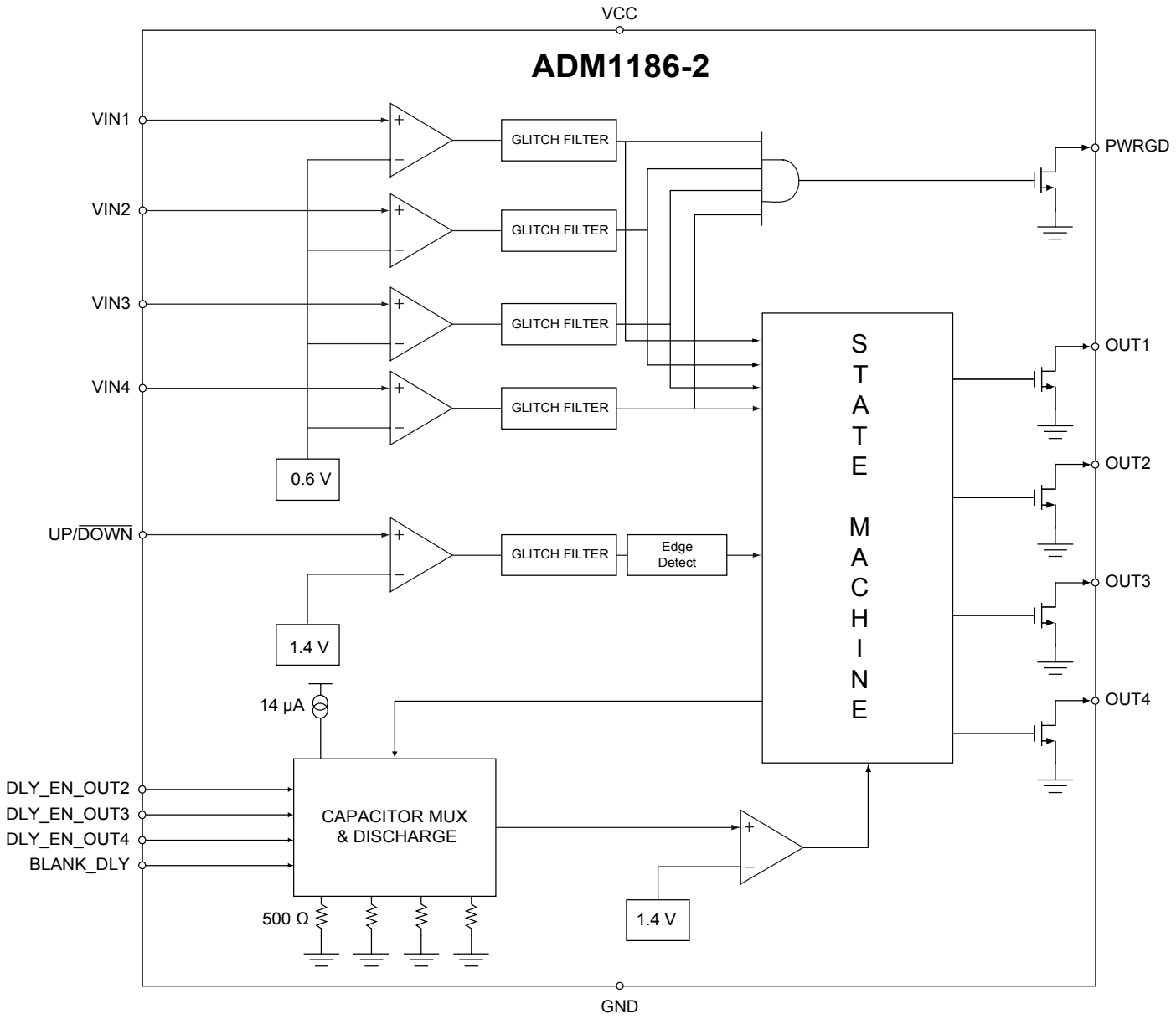



*Figure 22. Functional Block Diagram of the ADM1186-2*

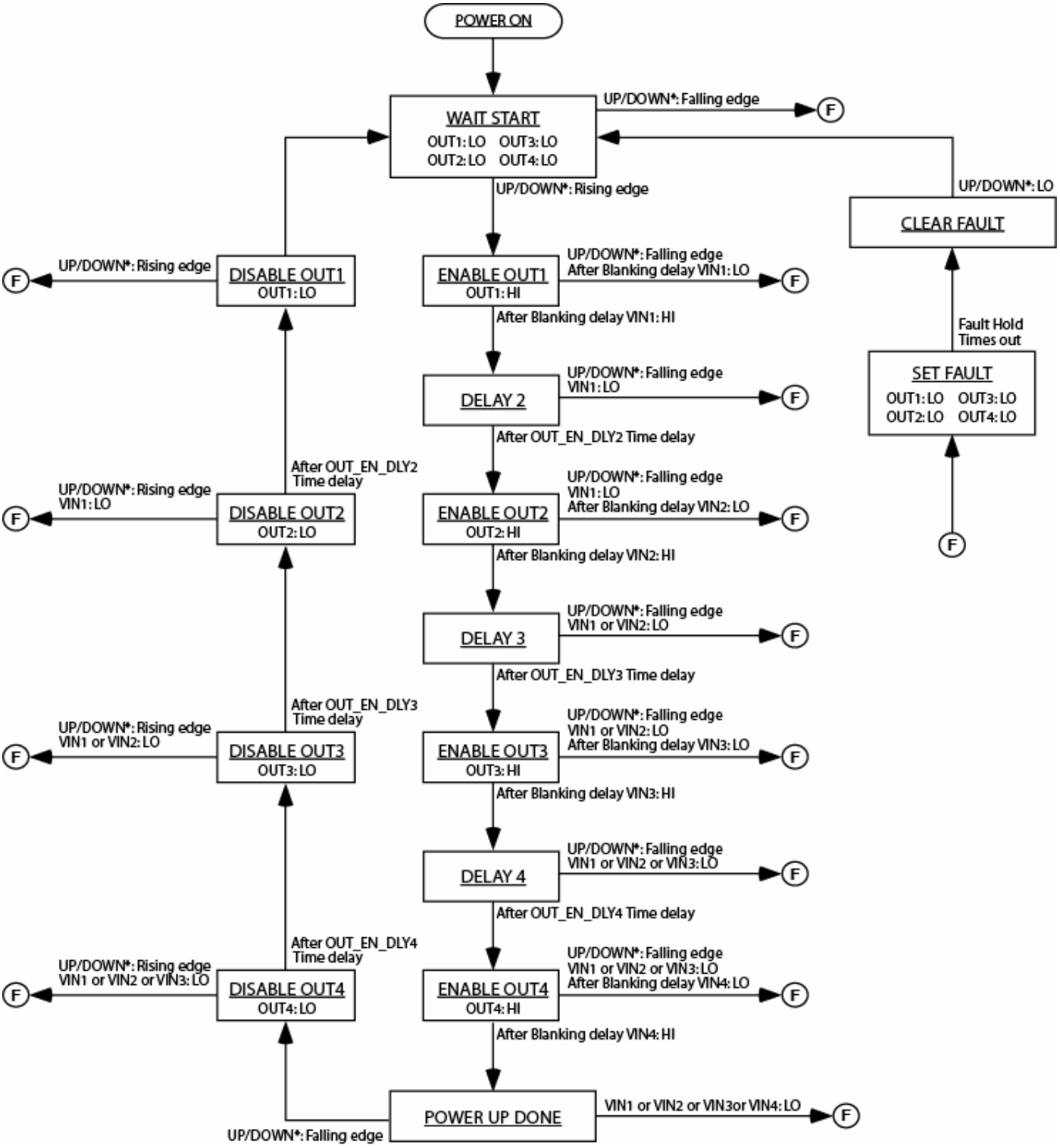
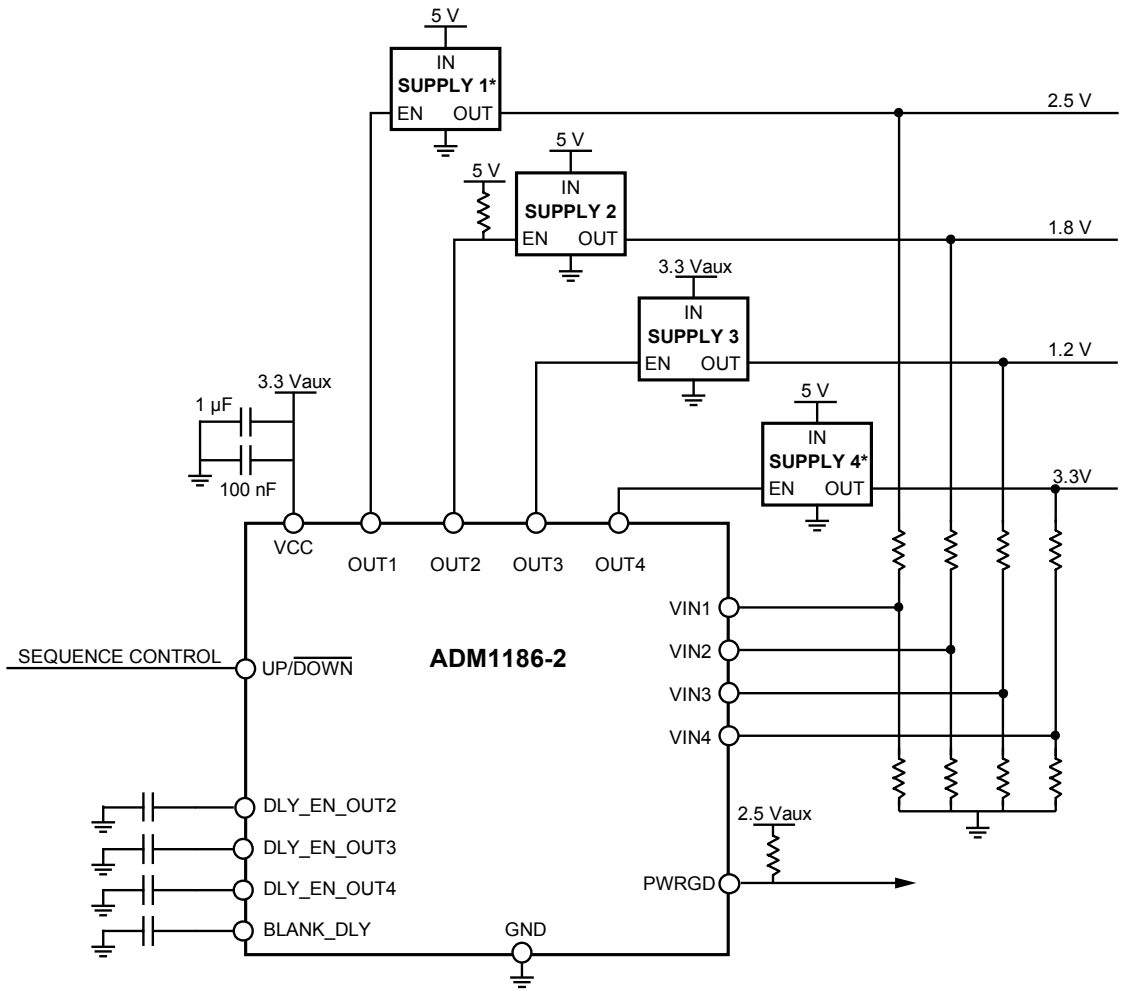



*Figure 23. ADM1186-2 State Machine Operation*




*Supplies 1,3 and 4 include an internal pull to their respective supplies.

*Figure 24.ADM1186-2 Typical Application*

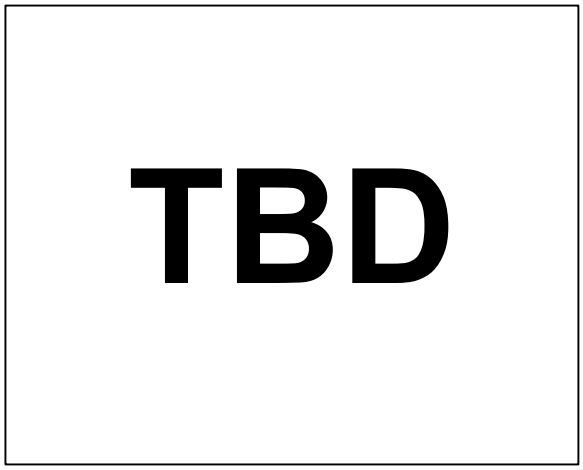



*Figure 25. Power-Up Waveforms*

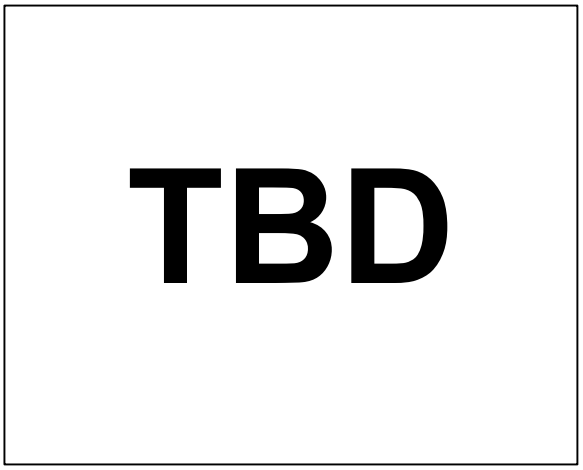



*Figure 26. Waveforms Showing Reaction to a Temporary Low Glitch on the Main Supply*

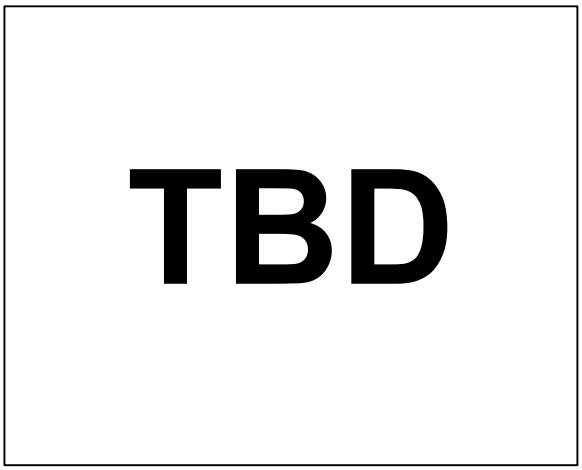



*Figure 27. Plot of OUTx and PWRGD Outputs at Startup in Applications Similar to Figure 3.*

## CASCADING MULTIPLE DEVICES

Multiple ADM1186-1 devices can be cascaded in applications that require more than four supplies to be sequenced and monitored. When cascaded, the controlled power up and down of all the cascaded supplies is maintained using just three pins on each device.

There are several configurations for interconnecting devices. The most suitable configuration depends on the application. Figure 28 and Figure 29 show two methods for cascading multiple ADM1186-1 devices.

Figure 28 shows a single sequence of twelve supplies. The capacitors used for timing are not shown for clarity. To ensure controlled up and down sequencing of all eight supplies the following connections are made:

- The UP pin of the first device and the $\overline{\text{DOWN}}$ pin of the last device in the cascade chain are connected together
- The SEQ_DONE pin of device N is connected to the UP pin of device N+1
- The SEQ_DONE pin of device N is connected to the $\overline{\text{DOWN}}$ pin of device N-1

When the SEQUENCE CONTROL line goes high, device A begins the power up sequence, turning on each enable in turn with the associated delays according to the state machine. When Device A completes the power up sequence, the SEQ_DONE signal goes from low to high, initiating a power up sequence on device B. When device B completes the power up sequence, the device B SEQ_DONE pin goes high, initiating a power up sequence on device C. When device C completes its power up sequence and all supplies are above the UV threshold then the system POWER GOOD signal goes high.

If the SEQUENCE CONTROL line goes low, device C starts a power down sequence, turning off its output enables. Once all of device C output enables are off the SEQ_DONE pin on device C goes low causing a high to low transition on the $\overline{\text{DOWN}}$ pin of device B. This initiates a power down sequence on device B, which takes all its OUTx pins low and then SEQ_DONE is taken low. This high to low transition is seen by device A and it starts its power down procedure completing the ordered shutdown of the twelve supplies.

Note: The capacitor on DLY_EN_OUT1 of device B (not shown in the figure) sets the sequence time delay between the last supply of device A and first supply of device B being turned on and off.

Figure 29 shows two independent sequences of four supplies each with common status outputs. In this case, both devices share the same sequence control signal so they start their power up/downs sequences together. Both devices must complete their power up sequences before the POWER GOOD signal goes high.

The $\overline{\text{FAULT}}$ pins of all devices in a cascade should be connected together. This ensures a fault on one device, or an unexpected event such as a rising or falling edge on the UP or $\overline{\text{DOWN}}$ pins will generate a fault condition on all other devices.

When a fault condition occurs on a device it pulls its $\overline{\text{FAULT}}$ line low. This in turns causes the other ADM1186 devices to pull their $\overline{\text{FAULT}}$ pins low in response in the SET FAULT state. Each device waits for the fault hold time to elapse and then moves to the CLEAR FAULT state.

A device in the CLEAR FAULT state holds its $\overline{\text{FAULT}}$ line low until its UP input pin is low. Then it moves into the WAIT ALL OK state and releases the $\overline{\text{FAULT}}$ line.

If, for example, a UV fault occurs during a power up sequence the UP pin will be high on the first device in the cascade. The first device in the cascade will hold $\overline{\text{FAULT}}$ low until the UP pin is brought low.

When this device releases the $\overline{\text{FAULT}}$ line, it allows all devices to move together from the WAIT ALL OK state back into the WAIT START state ready for the next power up sequence.

An external device such as a microcontroller, FPGA or an over-temperature sensor can cause a fault condition by bringing $\overline{\text{FAULT}}$ low, and the ADM1186-1 behaves as described. If the external device continues to hold the $\overline{\text{FAULT}}$ line low, the ADM1186-1 remains in the WAIT ALL OK state, effectively preventing the power up sequence from starting.

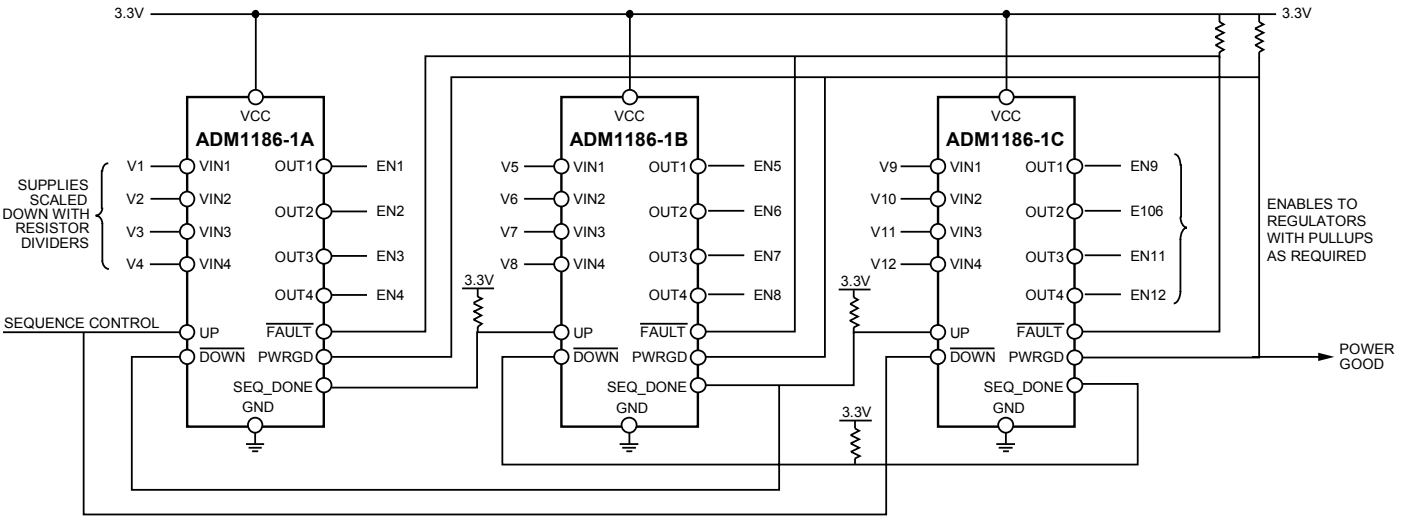



*Figure 28. Cascading Multiple ADM1186-1 Devices, Option 1*

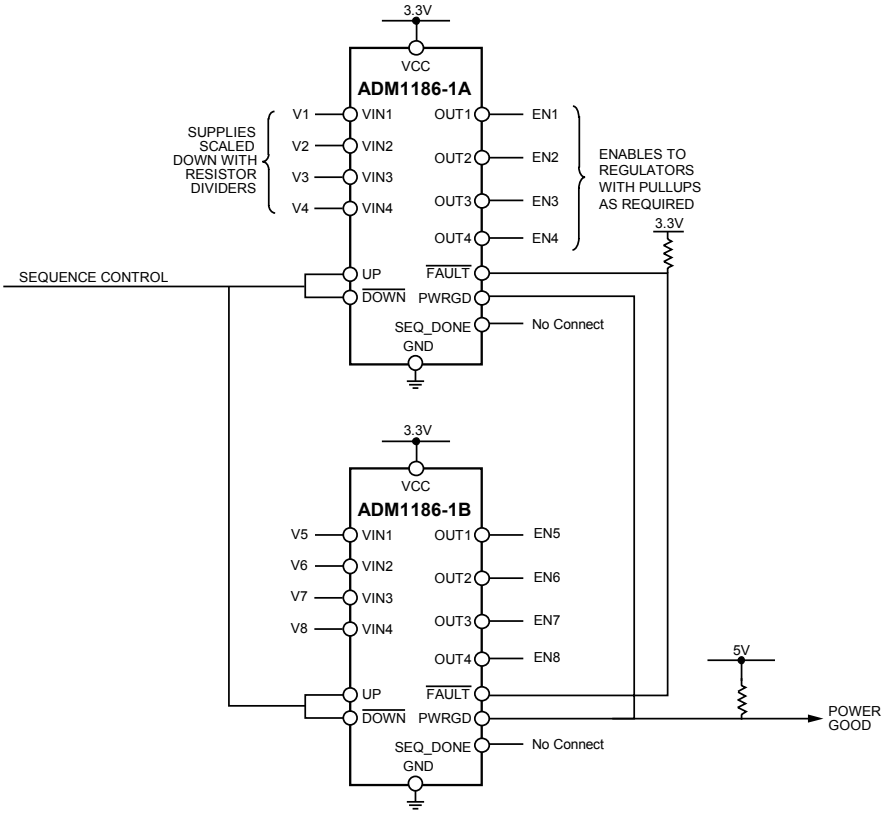
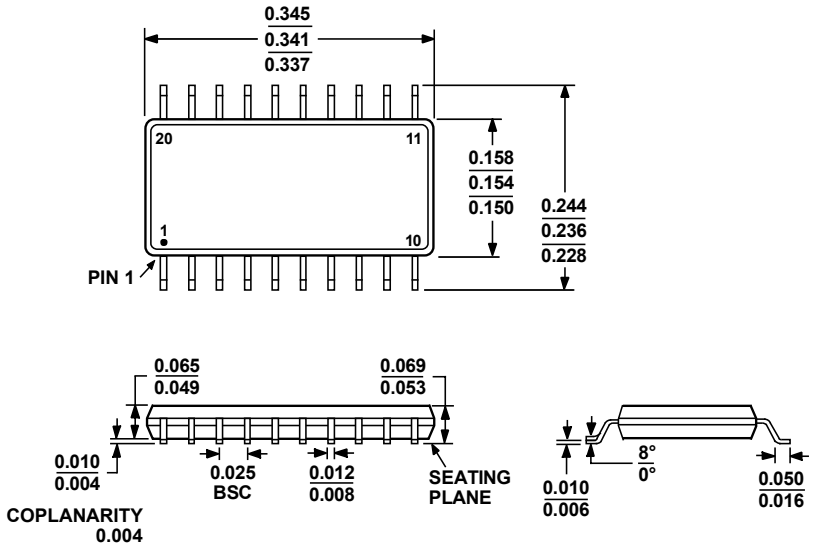


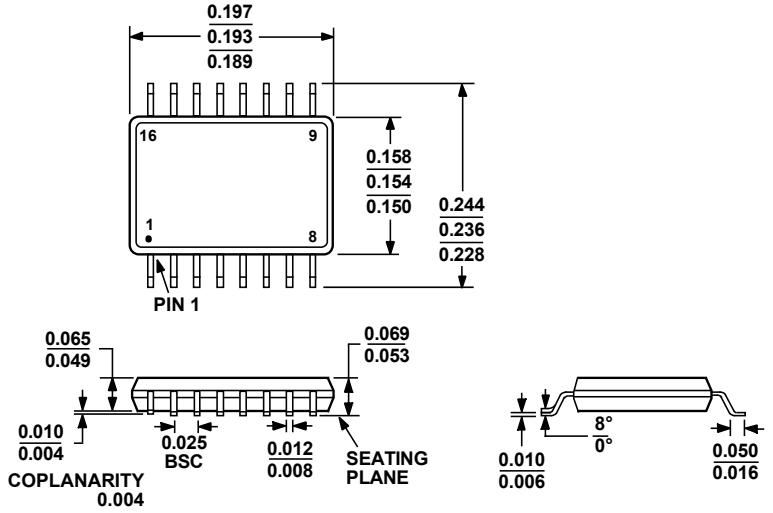

*Figure 29. Cascading Multiple ADM1186-1 Devices, Option 2*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-137-AD

*Figure 30. 20-Lead Shrink Small Outline Package [QSOP] (RQ-20)*
*Dimensions shown in inches*




COMPLIANT TO JEDEC STANDARDS MO-137-AB

*Figure 31. 16-Lead Shrink Small Outline Package [QSOP] (RQ-16)*
*Dimensions shown in inches*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Outline |
|---|---|---|---|
| ADM1186-1ARQZ[1] | −40°C to +85°C | 20-Lead Shrink Small Outline Package [QSOP] | RQ-20 |
| ADM1186-1ARQZ-REEL[1] | −40°C to +85°C | 20-Lead Shrink Small Outline Package [QSOP] | RQ-20 |
| ADM1186-2ARQZ[1] | −40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| ADM1186-2ARQZ-REEL[1] | −40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| EVAL-ADM1186-1EBZ[1] | | Evaluation Kit | |
| | | Micro-Evaluation Kit | |
| EVAL-ADM1186-2EBZ[1] | | Evaluation Kit | |
| | | Micro-Evaluation Kit | |

[1] Z = Pb-free part.

## NOTES


PR07153-0-10/07(PrJ)